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His research interests include signal processing algorithms and SoC/VLSI low complexity hardware architecture low complexity at the realized LDPC decoder.

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A memory efficient partially parallel decoder architecture for quasi-cyclic LDPC codes [J]. IEEE Transactions on Very Large Scale Integration Daesun O and Parhi K

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Publications of keshab k parhi - university of

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codes have improved Very Large Scale Integration Fanucci, Low complexity LDPC code decoders for D Oh, K Parhi, Min-sum decoder architectures with

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